SED1180

CMOS LCD 64-SEGMENT DRIVER

■ DESCRIPTION

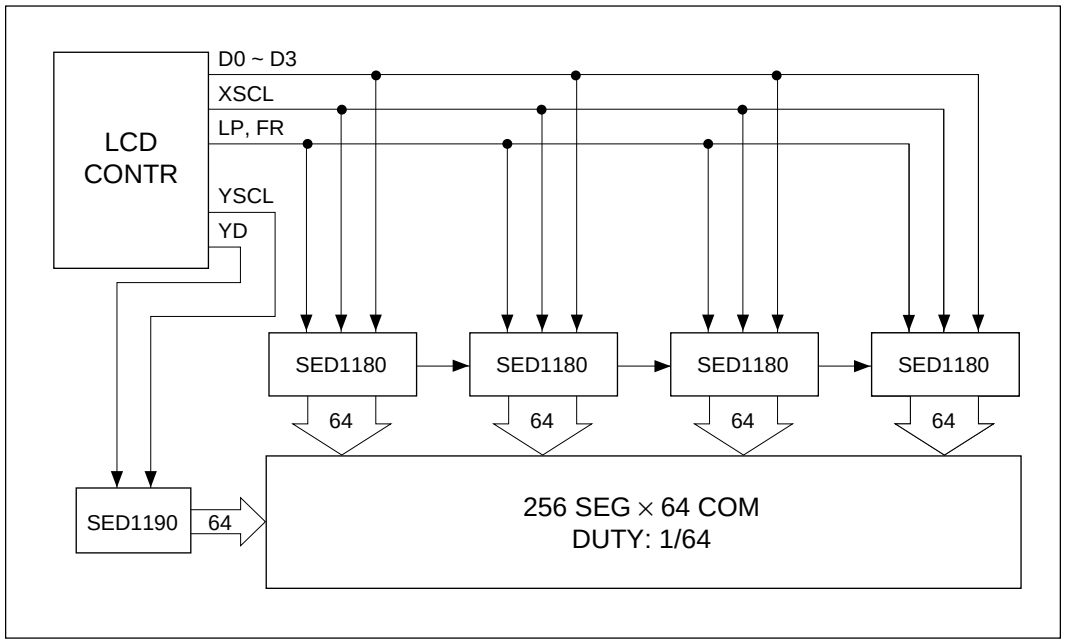
The SED1180 is a dot matrix LCD segment (column) driver for driving high-capacity LCD panel at duty cycles higher than 1/64. The LSI contains 64-bit shift register for display data. The display data is supplied through 4-bit bus, and serially transferred through 16 × 4 bit shift register. The display data is held in a 64-bit latch circuit. The LSI converts the level of the latched data to an LCD drive waveform.

The SED1180 is used in conjunction with the SED1190 (64-bit row driver) to drive a large-capacity dot matrix LCD panel.

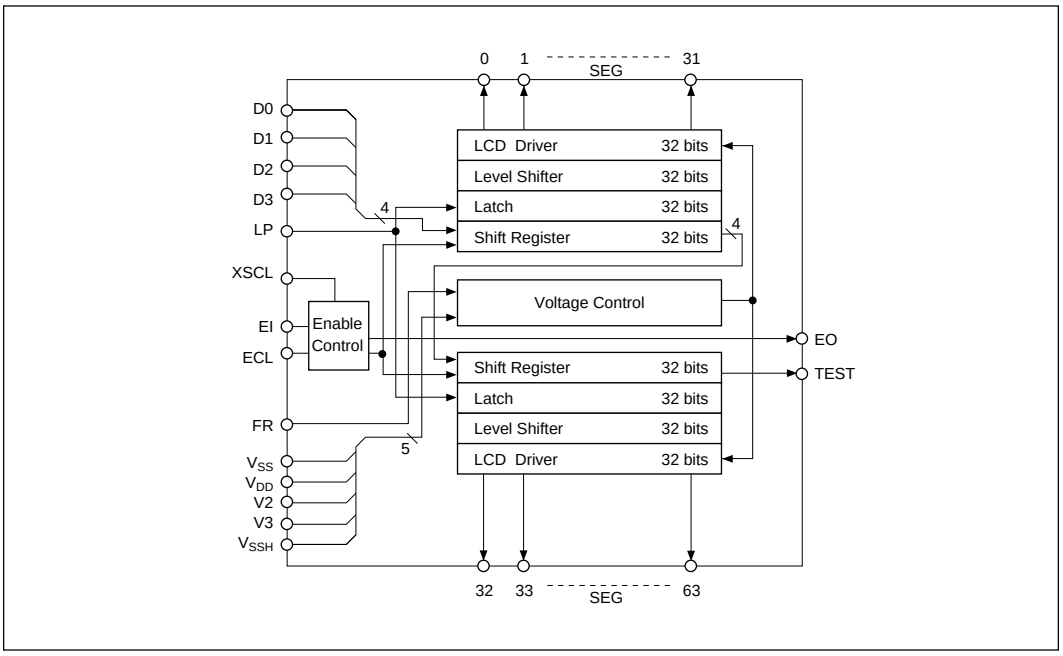
■ FEATURES

- Low-power CMOS technology
- 64-bit segment (column) driver
- High-speed 4-bit data
- Duty cycle ..... 1/64 to 1/128
- Daisy chain enable support
- Wide range of LCD voltage ..... –14V to –25V
- Supply voltage ..... 5.0V ±10%
- Package ..... QFP1-80 pin (F_{0A})
  QFP5-80 pin (F_{5A})
  DIE: Al pad chip (D_{0A})

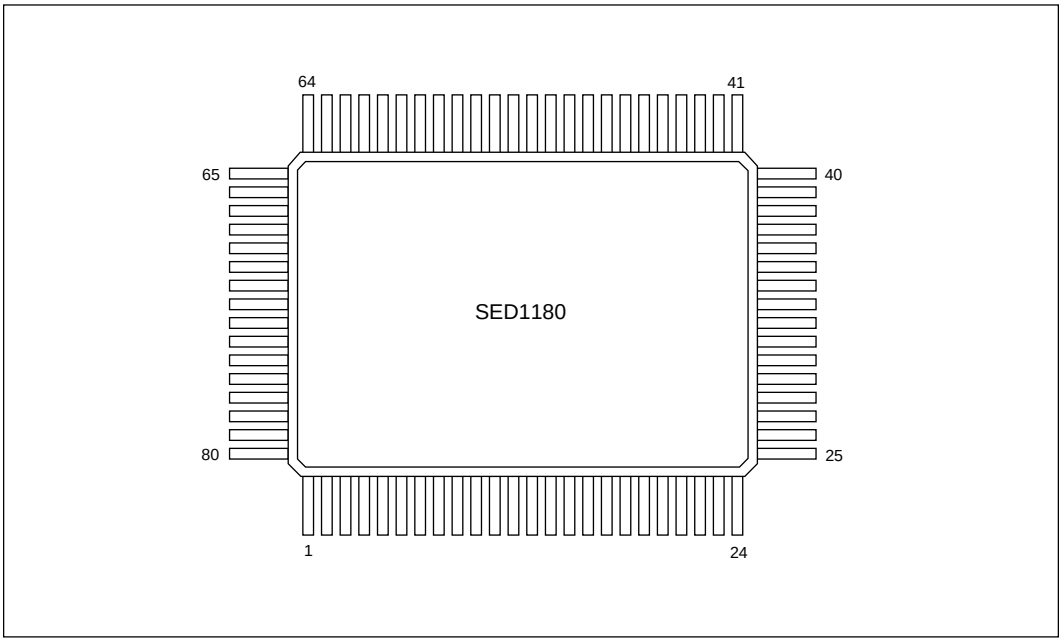
■ SYSTEM BLOCK DIAGRAM



■ BLOCK DIAGRAM



■ PIN CONFIGURATION



Number	Name	Number	Name	Number	Name	Number	Name
1	SEG27	21	SEG 7	41	SEG36	61	SEG56
2	SEG26	22	SEG 6	42	SEG37	62	SEG57
3	SEG25	23	SEG 5	43	SEG38	63	SEG58
4	SEG24	24	SEG 4	44	SEG39	64	SEG59
5	SEG23	25	SEG 3	45	SEG40	65	SEG60
6	SEG22	26	SEG 2	46	SEG41	66	SEG61
7	SEG21	27	SEG 1	47	SEG42	67	SEG62
8	SEG20	28	SEG 0	48	SEG43	68	SEG63
9	SEG19	29	EO	49	SEG44	69	V_{SSH}
10	SEG18	30	D3	50	SEG45	70	V2
11	SEG17	31	D2	51	SEG46	71	V3
12	SEG16	32	D1	52	SEG47	72	V_{SS}
13	SEG15	33	D0	53	SEG48	73	V_{DD}
14	SEG14	34	XSCL	54	SEG49	74	TEST
15	SEG13	35	LP	55	SEG50	75	EI
16	SEG12	36	FR	56	SEG51	76	ECL
17	SEG11	37	SEG32	57	SEG52	77	SEG31
18	SEG10	38	SEG33	58	SEG53	78	SEG30
19	SEG 9	39	SEG34	59	SEG54	79	SEG29
20	SEG 8	40	SEG35	60	SEG55	80	SEG28

■ PIN DESCRIPTION

Pin Name	Function
SEG0 to SEG63	Outputs to segment pins of LCD. Output level changes at each latch pulse LP falling edge.
XSCL	Data shift clock input: display data is shifted in on the falling edge of this signal.
LP	Latch pulse for displayed data, falling edge trigger: display data is latched on the falling edge of this signal.
FR	LCD AC-drive signal
EI	Active high daisy chain enable input
EO	Active high daisy chain enable output
ECL	Daisy chain enable clock: the daisy chain enable is propagated on the falling edge of this clock.
D0 to D3	4-bit display data input
TEST	Test output
V_{DD}, V_{SS}	Logic power inputs
V2, V3, V_{SSH}	LCD drive power inputs V_{SSH}: –14V to –23V $V_{DD} \geq V2 \geq V3 \geq V_{SSH}$

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Ratings	Unit
Supply voltage (1)	V_{SS}	–7.0 to +0.3	V
Supply voltage (2)	V_{SSH}	–28.0 to +0.3	V
	V_2, V_3		
Input voltage	V_I	V_{SS} – 0.3 to +0.3	V
Operating temperature	T_{opr}	–20 to +75	°C
Storage temperature	T_{stg}	–55 to +125	°C
Soldering temperature time	T_{sol}	260°C, 10 sec (at lead)	—

Notes:

1. All voltage measurements are based on V_{DD} = 0V.
2. V2 and V3 must always satisfy the condition $V_{DD} \geq V2, V3 \geq V_{SSH}$.
3. Exceeding the absolute maximum ratings can result in permanent damage to the device. Functional operation under these conditions is not implied.
4. Moisture resistance of flat packages can be reduced by the soldering process. Care should be taken to avoid thermally stressing the package during board assembly.

■ ELECTRICAL CHARACTERISTICS

● DC Electrical Characteristics

(V_{DD} = 0V, V_{SS} = –5.0 V ± 10%, T_a = –20 to 75°C)

Parameters	Symbol	Condition		Rating			Unit
				Min	Typ	Max	
Supply voltage (1)	V_{SS}			–5.5	–5.0	–4.5	V
Supply voltage (2)	V_2			V_{SSH}	—	V_{DD}	V
	V_3			V_{SSH}	—	V_{DD}	V
	V_{SSH}	Recommended V_{SSH}		–25.0	—	–14.0	V
		Operable V_{SSH} (see note)		–25.0	—	–5.0	V
HIGH-level input voltage	V_{IH}			0.2V_{SS}	—	V_{DD}–0.3	V
LOW-level input voltage	V_{IL}			V_{SS}–0.3	—	0.8V_{SS}	V
HIGH-level output voltage	V_{OH}	I_{OH} = -0.6 ma		-0.4	—	—	V
LOW-level output voltage	V_{OL}	I_{OL} = 0.6 ma		—	—	V_{SS}+0.4	V
Input leakage current	I_{LI}	0 V ≤ V_I ≤ V_{SS}		—	0.05	2.0	µA
Output leakage current	I_{LO}	0 V ≤ V_O ≤ V_{SS}		—	0.05	5.0	µA
Shift clock	XSCL			—	—	6.0	MHz
Frame signal	FR			—	1/60	—	S
Input capacitance	C_I	T_a = 25°C		—	5.0	8.0	pF
Segment output on resistance	R_{SEG}	V_{OH} = V_{DD} = –0.5 V V_{OL} = V_{SSH} = +0.5 V SEG bit	V_{SSH} = –20.0 V	—	1.9	2.9	kΩ
			V_{SSH} = –14.0 V	—	2.4	3.9	
			V_{SSH} = –9.0 V	—	3.6	7.0	
			V_{SSH} = –5.0 V	—	11.5	500.0	
Quiescent current	I_Q	V_{SSH} = –25 V, V_{SSH} = –5.5 V, V_I = V_{DD}		—	0.05	30	µA
Operating current for the logic	I_{SSO}	FR cycle = 16.7 ms ECL cycle = 13 µS	V_{SS} = –5.0 V, V_{IH} = V_{DD}, V_{IL} = V_{SS}, LP cycle=130 µS, XSCL=1.5 MHz, (duty 50%) All data input reversed bit by bit. All output pins are open.	—	90	200	µA
Operating current for the LCD	I_{SSHO}	FR cycle = 16.7 ms ECL cycle = 13 µS	V_{SS} = –4.5 V, V_2 = –4.0 V, V_1 = –16.0 V, V_{SSH} = –20.0 V, V_{IH} = V_{DD}, V_{IL} = V_{SS}, XSCL=1.5 MHz, (duty 50%), all data input reversed bit by bit. All output pins are open.	—	40	80	µA

(continued)

- **DC Electrical Characteristics (continued)**

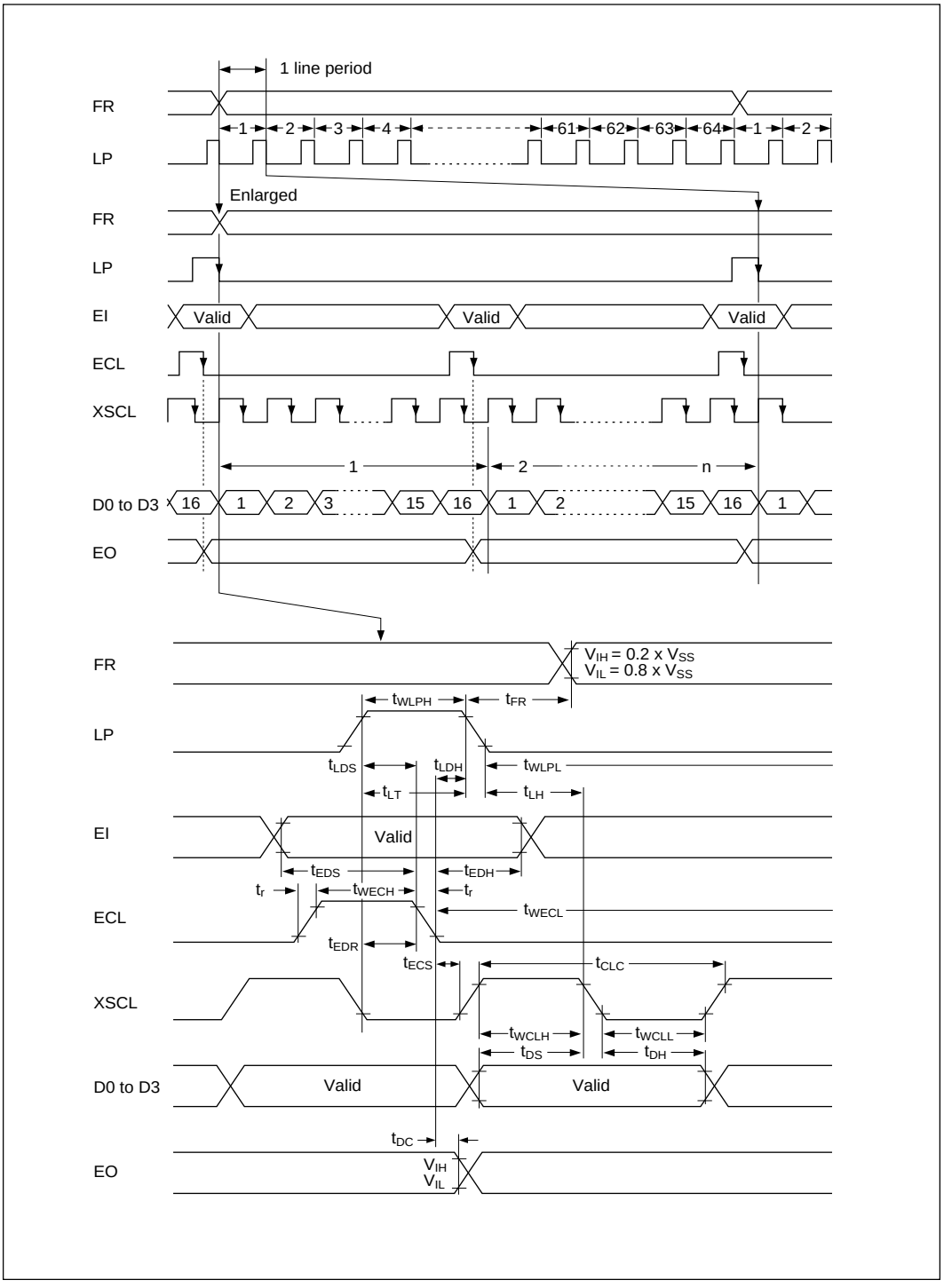
Parameters	Symbol	Condition	Rating			Unit
			Min	Typ	Max	
Shift clock cycle	t_{CLC}		166	—	—	ns
Shift clock “H” width	t_{WCLH}		63	—	—	ns
Shift clock “L” width	t_{WCLL}		63	—	—	ns
Data setup time	t_{DS}		50	—	—	ns
Data hold time	t_{DH}		30	—	—	ns
Enable clock “H” width	t_{WECH}	See note 4	100	—	—	ns
Enable clock “L” width	t_{WECL}	See note 4	100	—	—	ns
Enable data setup time	t_{EDS}	See note 4	50	—	—	ns
Enable data hold time	t_{EDH}	See note 4	20	—	—	ns
Enable clock delay time	t_{EDR}	See note 4	–10	—	—	ns
Enable clock setup time	t_{ECS}	See note 4	70	—	—	ns
Latch pulse “H” width	t_{WLPH}	See note 2	110	—	—	ns
Latch pulse “L” width	t_{WLPL}		220	—	—	ns
Latch timing	t_{LT}		100	—	—	ns
Latch hold time	t_{LH}		0	—	—	ns
Latch pulse data setup time	t_{LDS}	See notes 3 & 4	140	—	—	ns
Latch pulse data hold time	t_{LDH}	See notes 3 & 4	50	—	—	ns
Permissible frame signal delay	t_{DFR}		–500	—	500	ns
Input signal rise time	t_r		—	—	See note 4	—
Input signal fall time	t_f		—	—	See note 4	—
Enable output delay	t_{PD}	See note 4	20	—	150	ns

Notes:

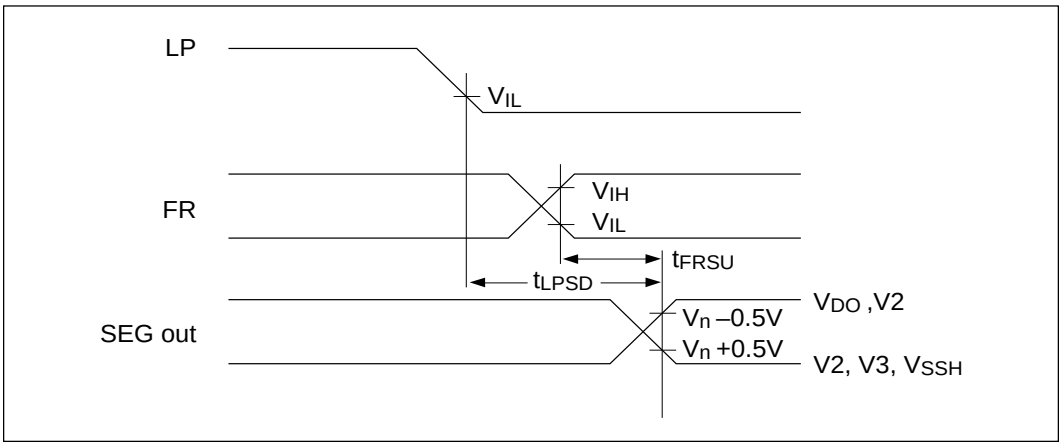
1. While the drive is guaranteed to operate without error within this voltage range, the output resistance of the segment drivers will be higher than that in the recommended operating range. It is suggested that the drive capability of the driver under these conditions is tested using the target panel.
2. t_{WLPH} = 160 ns (min) when LP is used as EI data.
3. t_{WLPH} = 250 ns (min) when EO is reset by LP.
4. Applies to the SED1180F only.
5. t_r, $t_f < (t_{CLC} – t_{WCLH} – t_{WCLL}) / 2$ and t_r, $t_f \leq 50$ ns.

■ AC ELECTRICAL CHARACTERISTICS

● Data I/O Timing



- **Segment Drive Timing**

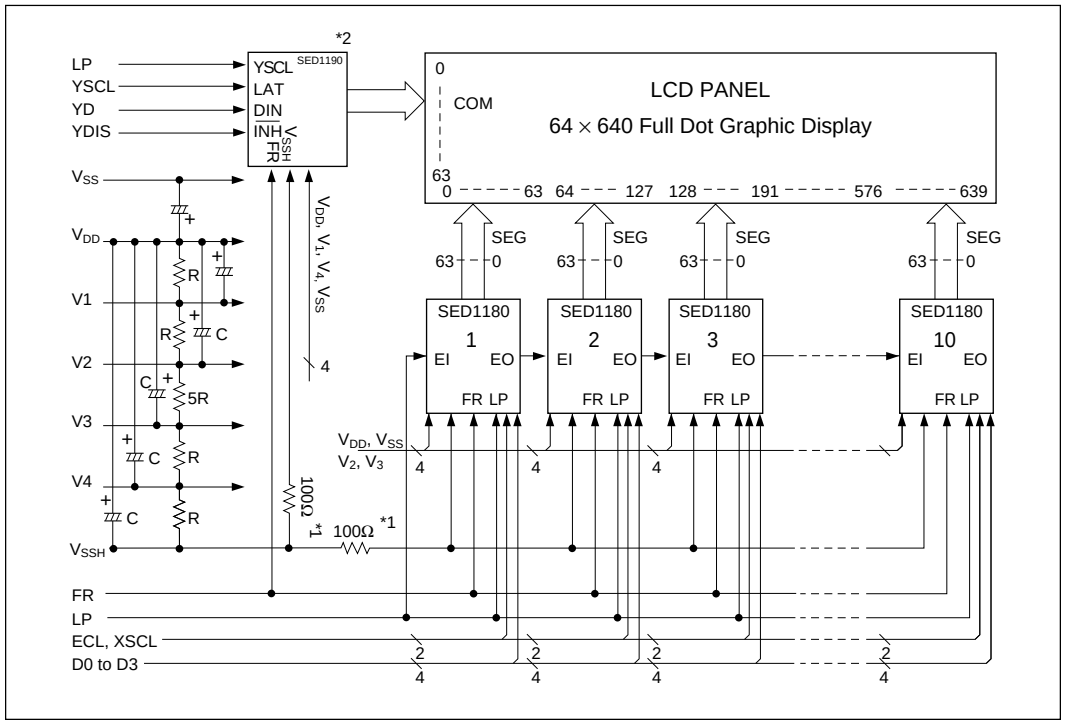


V_{IH} = 0.2V_{SS}; V_{IL} = 0.8V_{SS} (V_{DD} = 0V, V_{SS} = –5.0 V ±10%, T_a = –20 to 75°C)

Parameters	Symbol	Condition	Rating			Unit
			Min	Typ	Max	
LP-SEG output delay time	t_{LPSD}	V_{SSH}=–14.0 to –25.0 V,	—	—	4.5	µs
FR-SEG output delay time	t_{FRSD}	C_L= 100 pF	—	—	4.5	µs

■ TYPICAL SYSTEM CONNECTION

(64 × 640 pixels, 1/64 duty ratio)



Notes:

1. Current limiting resistors
2. Bypass V_{SS} and V_{SSH} with capacitors of at least 0.01 μF

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