SED1190

CMOS LCD 64-COMMON DRIVERS

■ DESCRIPTION

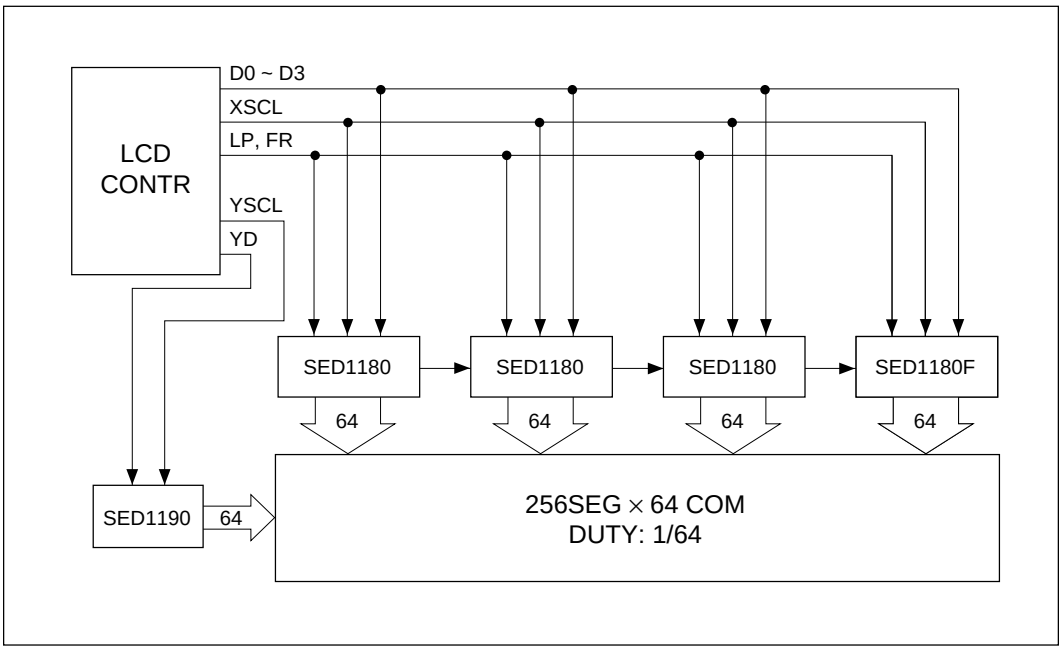
The SED1190 is a dot matrix LCD common (row) driver for driving high-capacity LCD panel at duty cycles higher than 1/64. The LSI uses two serially connected, 32-bit shift registers to hold the display data, and level shifter converts the TTL level 64-bit parallel data from the shift registers to levels suitable for use by the LCD drive circuitry. The SED1190 generates common drive signals using the voltages supplied to LCD drive voltages pins.

The SED1190 is used in conjunction with the SED1180 (64-bit row driver) to drive a large capacity dot matrix LCD panel.

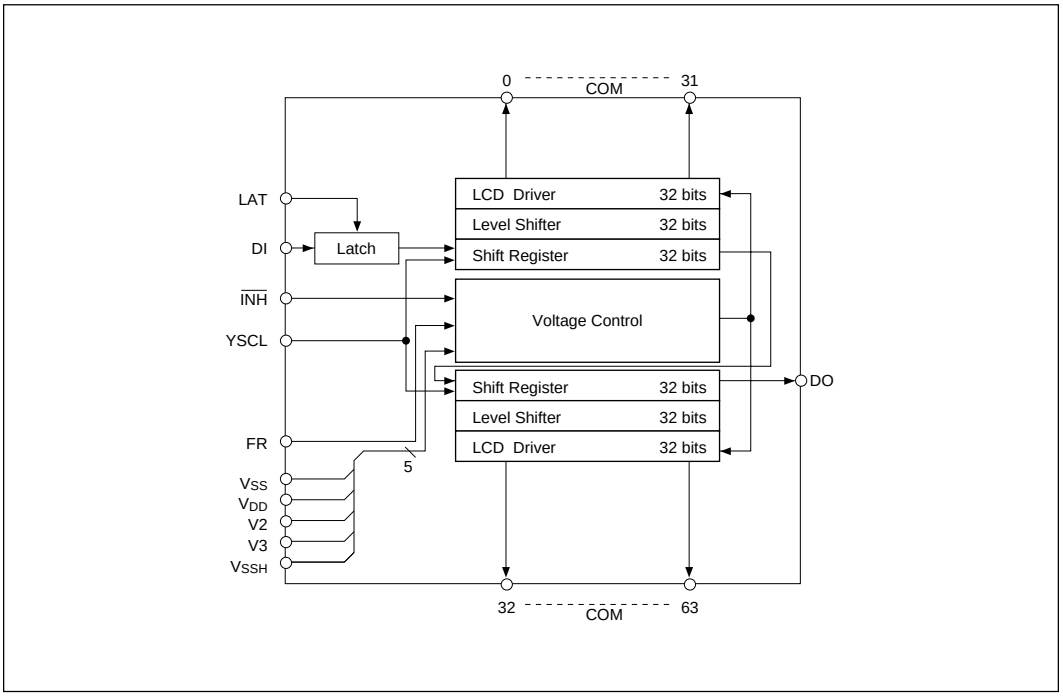
■ FEATURES

- Low-power CMOS technology
- 64-bit common (row) driver
- Display blanking
- Duty cycle: 1/64 to 1/128
- Daisy chain enable support
- Wide range of LCD voltage: –14V to –25V
- Supply voltage: 5.0V ±10%
- Package: ..... QFP1-80 pin (F_{0A})
  QFP5-80 pin (F_{5A})
  DIE: Al pad chip (D_{0A})

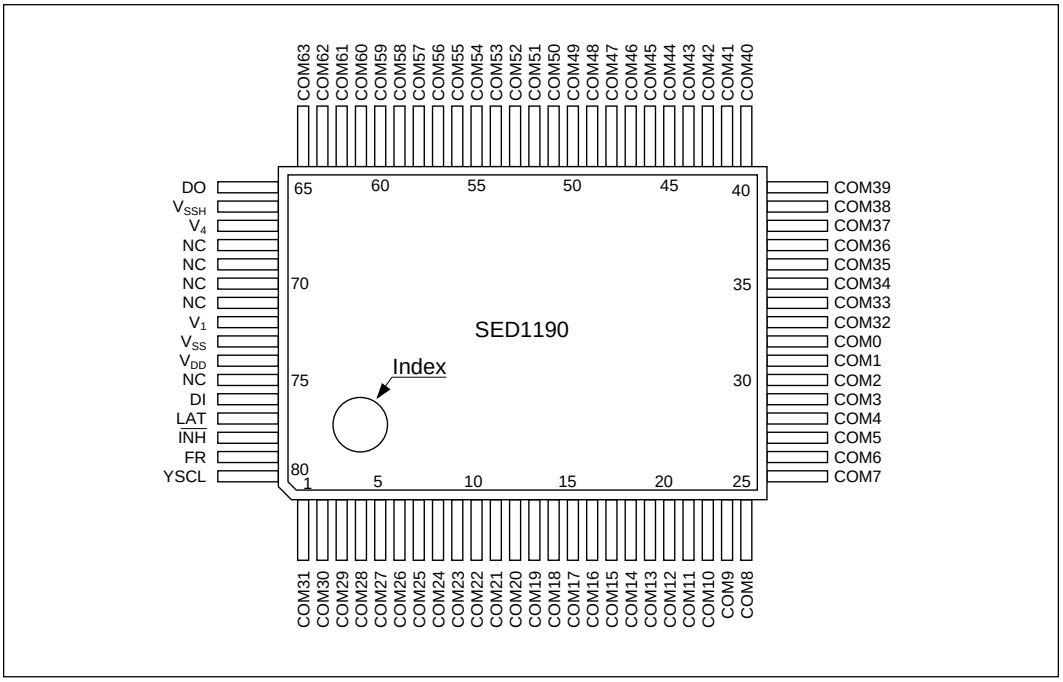
■ SYSTEM BLOCK DIAGRAM



■ BLOCK DIAGRAM



■ PIN CONFIGURATION



Number	Name	Number	Name	Number	Name	Number	Name
1	COM31	21	COM11	41	COM40	61	COM60
2	COM30	22	COM10	42	COM41	62	COM61
3	COM29	23	COM 9	43	COM42	63	COM62
4	COM28	24	COM 8	44	COM43	64	COM63
5	COM27	25	COM 7	45	COM44	65	DO
6	COM26	26	COM 6	46	COM45	66	V_{SSH}
7	COM25	27	COM 5	47	COM46	67	V4
8	COM24	28	COM 4	48	COM47	68	NC
9	COM23	29	COM 3	49	COM48	69	NC
10	COM22	30	COM 2	50	COM49	70	NC
11	COM21	31	COM 1	51	COM50	71	NC
12	COM20	32	COM 0	52	COM51	72	V1
13	COM19	33	COM32	53	COM52	73	V_{SS}
14	COM18	34	COM33	54	COM53	74	V_{DD}
15	COM17	35	COM34	55	COM54	75	NC
16	COM16	36	COM35	56	COM55	76	DI
17	COM15	37	COM36	57	COM56	77	LAT
18	COM14	38	COM37	58	COM57	78	$\overline{INH}$
19	COM13	39	COM38	59	COM58	79	FR
20	COM12	40	COM39	60	COM59	80	YSCL

NC = Not connected

■ PIN DESCRIPTION

Pin Name	Function
COM0 to COM63	LCD common drive outputs
DI	Serial data input
LAT	Transparent latch control input: LAT / DI / DI latch output H / H / H H / L / L L / X / DI latch
DO	Serial data output
YSCL	Serial data shift clock. Data is shifted through the controller on the falling edge of this clock
FR	LCD AC-drive signal input
$\overline{INH}$	Active-low blanking input
V_{DD}, V_{SS}	Logic power supply inputs
V1, V4, V_{SSH}	LCD drive power inputs $V_{DD} \geq V1 \geq V4 \geq V_{SSH}$

■ ELECTRICAL CHARACTERISTICS

● Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Supply voltage (1)	V_{SS}	–7.0 to +0.3	V
Supply voltage (2)	V_{SSH}	–28.0 to +0.3	V
	V1, V4		
Input voltage	V_I	V_{SS} –0.3 to +0.3	V
Operating temperature	T_{opr}	–20 to +75	°C
Storage temperature	T_{stg}	–55 to +125	°C
Soldering temperature and time	T_{sol}	260, 10	°C, s

Notes:

1. All voltages referenced to a V_{DD} of 0 V.
2. V1 and V4 must satisfy the relationship $V_{DD} \geq V1, V4 \geq V_{SSH}$
3. Exceeding the absolute maximum ratings can cause permanent damage to the device. Functional operation under these conditions is not implied.
4. Moisture resistance of flat packages can be reduced by the soldering process. Care should be taken to avoid thermally stressing the package during board assembly.

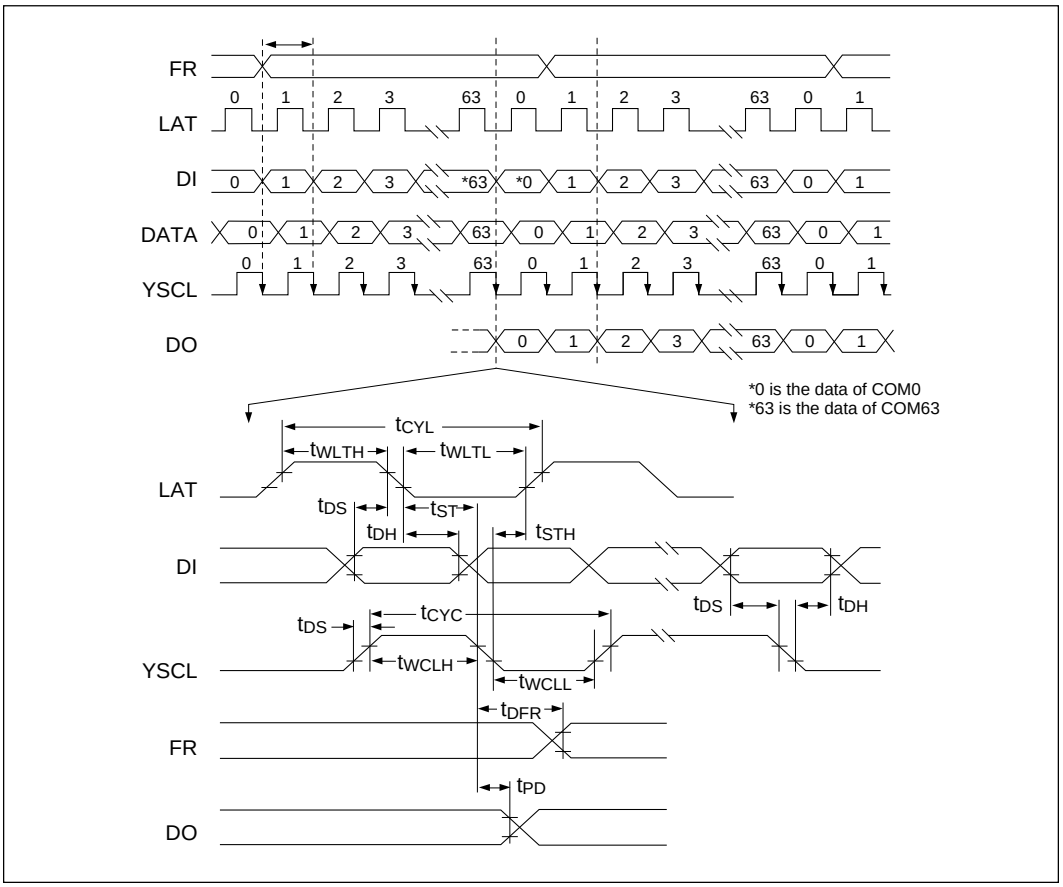
- **DC Characteristics**

(V_{DD} = 0V, V_{SS} = –5.0 V ±10%, T_a = –20 to 75°C)

Parameter	Symbol	Conditions		Rating Min	Rating Typ	Rating Max	Unit
Supply voltage (1)	V_{SS}			–5.5	–5.0	–4.5	V
Supply voltage (2)	V1			V_{SSH}	—	V_{DD}	V
	V4			V_{SSH}	—	V_{DD}	V
	V_{SSH}	Recommended V_{SSH}		–25.0	—	–14.0	V
		Operable V_{SSH} (see note)		–25.0	—	–5.0	V
High level input voltage	V_{IH}			0.2V_{SS}	—	V_{DD}+0.3	V
Low level input voltage	V_{IL}			V_{SS}–0.3	—	0.8V_{SS}	V
High level output voltage	V_{OH}	I_{OH} = –0.6 mA		–0.4	—	—	V
Low level output voltage	V_{OL}	I_{OL} = 0.6 mA		—	—	V_{SS}+0.4	V
Input leakage current	I_{LI}	0 V ≥ V_I ≥ V_{SS}		—	0.05	2.0	µA
Output leakage current	I_{LO}	0 V ≥ V_O ≥ V_{SS}		—	0.05	5.0	µA
Shift clock	YSCL			—	—	2.5	MHz
Frame signal	FR			—	1/60	—	s
Input capacitance	C_I	T_a = 25°C		—	5.0	8.0	pF
Common output on resistance	R_{COM}	V_{OH} = V_{DD} –0.5 V V_{OL} = V_{SSH} +0.5 V COM bit	V_{SSH} = –20.0 V	—	0.8	1.0	kΩ
			V_{SSH} = –14.0 V	—	0.9	1.3	
			V_{SSH} = –9.0 V	—	1.3	2.0	
			V_{SSH} = –5.0 V	—	3.0	30.0	
Quiescent current	I_Q	SED 1190	V_{SSH} = –25 V, V_{SSH} = –5.5 V, V_I = V_{DD}	—	0.05	30	µA
Operating current for the logic	I_{SS}	FR cycle = 16.7 ms	V_{SS} = –5.0 V, V_{IH} = V_{DD}, V_{IL} = V_{SS}, YSCL cycle = 130 µs (duty 50%), All "H" output terminals are opened at every data input all 1/128 duty.	—	3.0	8.0	µA
Operating current for LCD	I_{SSH}	FR cycle = 16.7 ms	V_{SS} = –4.5 V, V_1 = –2.0 V, V_4 = –18.0 V, YSCL cycle = 130 µs (duty 50%), All "H" output terminals are opened at every data input of 1/128 duty.	—	3.0	8.0	µA
Pull up MOS current	$–I_p$	V_{SS} = –5.0 V, V_{IL} = –5.0 V Applicable to LAT input terminals		10.0	25.0	50.0	µA

Note: Error free operation is guaranteed in this range but the output resistance of the LCD drivers is higher than in the recommended operating range. It is suggested that the driver is tested with the target LCD panel to determine if performance is acceptable.

- **AC Electrical Characteristics**
  - **I/O Signal Timing**

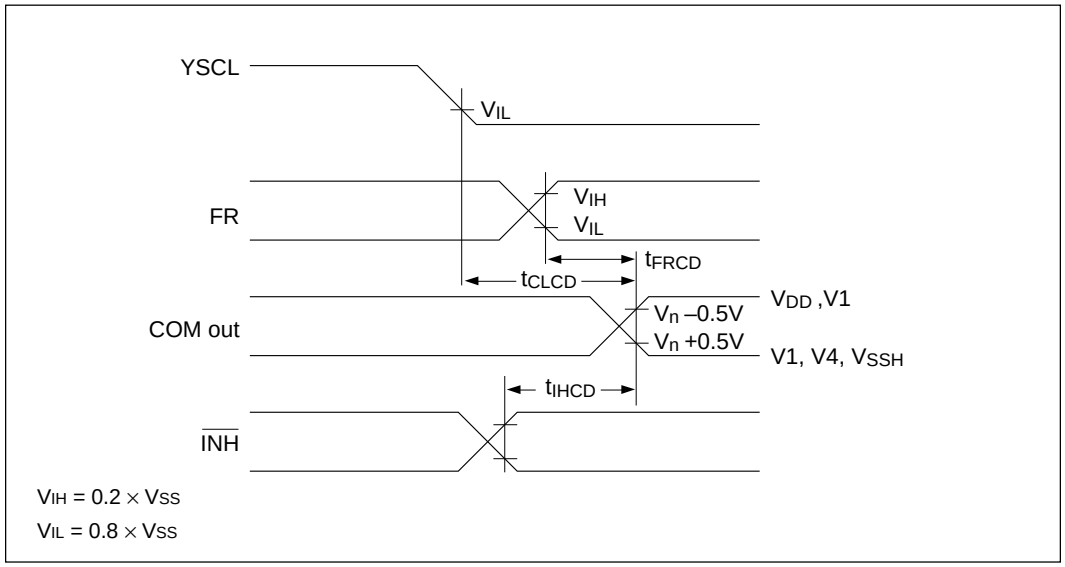


V_{DD} = 0V, V_{SS} = –5.0V ± 10%, T_a = –20 to 75°C

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Latch pulse cycle time	t_{CYL}	—	400	—	—	ns
Latch pulse “H” width	t_{WLTH}	—	180	—	—	ns
Latch pulse “L” width	t_{WLL}	—	180	—	—	ns
Shift clock cycle time	t_{CYC}	—	400	—	—	ns
Shift clock “H” time	t_{WCLH}	—	110	—	—	ns
Shift clock “L” time	t_{WCLL}	—	110 (240)	—	—	ns
Data setup time	t_{DS}	—	100 (70)	—	—	ns
Data hold time	t_{DH}	—	30	—	—	ns
Data shift timing	t_{ST}	—	0	—	—	ns
Data shift hold time	t_{STH}	—	125	—	—	ns
Permissible frame signal delay	t_{DFR}	—	–500	0	500	ns
Input signal rise time	t_r	—	—	—	*	ns
Input signal fall time	t_f	—	—	—	*	ns
Data output delay time	t_{pD}	C_L = 15pF	30	—	170	ns

* t_r, t_f = (t_{CYL} – t_{WLH} – t_{WLTL}) / 2 where tf ≥ 50ns.

● **Common Drive**

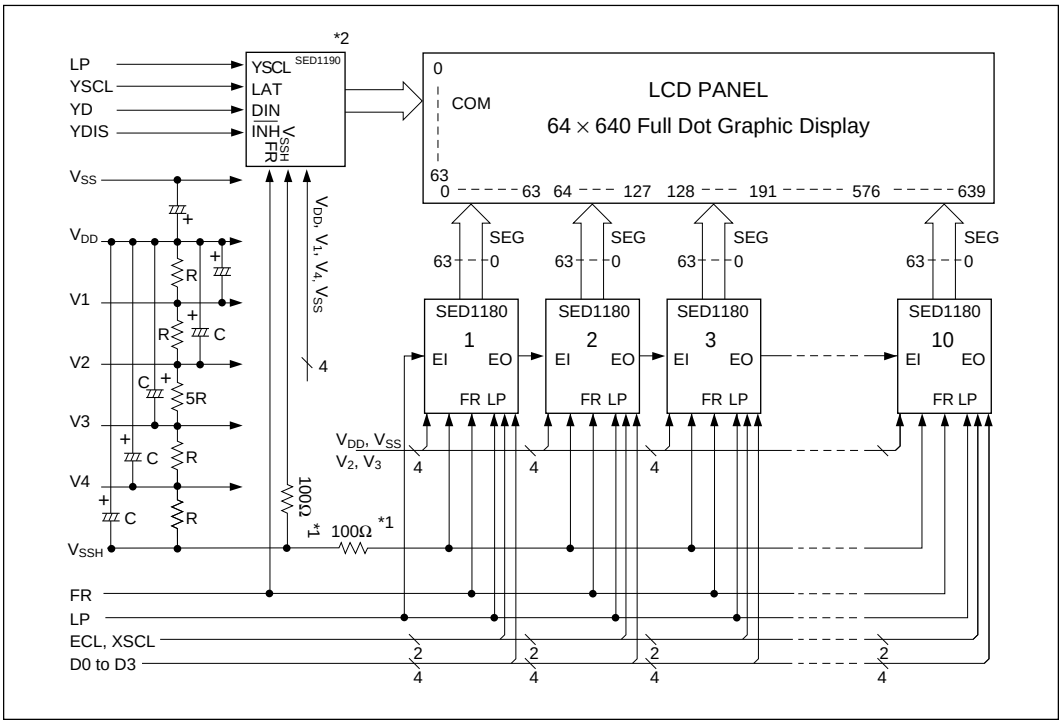


V_{DD} = 0V, V_{SS} = –5.0V ± 10%, T_a = –20 to 75°C

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
YSCL – COM output delay time	t_{CLCD}	V_{SSH} = –14.0 to –25.0V C_L = 100pF	—	—	3.0	µs
RF – COM output delay time	t_{FRCD}		—	—	3.0	µs
INH – COM output delay time	t_{IHCD}		—	—	3.0	µs

■ EXAMPLE OF APPLICATION

(64 × 640 pixels, 1/64 duty ratio)



Notes:

1. Current limiting resistors
2. Bypass V_{SS} and V_{SSH} with capacitors of at least 0.01 μF